# Design and Analysis of Hybrid Multilevel Inverter for Asymmetrical Input Voltage

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**Abstract.** [1]The project begins by delving into the foundational concepts of multilevel inverters, highlighting their advantages over traditional inverters.[2]Leveraging techniques discussed, the project explores advanced control strategies and modulation techniques crucial for optimizing performance in asymmetrical input voltage scenarios.[3]Insights from industrial applications inform the discussion on design considerations tailored to industrial settings, addressing challenges posed by asymmetrical input voltages.[4] Building upon previous research, the project investigates robust control algorithms essential for effectively managing asymmetrical voltage fluctuations, particularly in renewable energy systems.[5]The project examines the integration of the latest advancements in power semiconductor devices into multilevel inverter designs, considering implications for efficiency under asymmetrical voltage conditions. [6]Techniques outlined are employed to develop accurate models and simulation methodologies for analysing the performance of multilevel inverters under varying input voltage conditions. [7]Drawing insights from grid-connected photovoltaic power generation, the project explores the integration of multilevel inverters into grid-connected photovoltaic systems, focusing on adaptation to asymmetrical input voltages from solar arrays.[8] Lastly, the project examines the critical role of multilevel inverters in grid stability and renewable energy integration.

***Keywords* -** Diode clamped inverter, T-type leg, Hybrid multilevel inverter, Asymmetric source, MOSFET, Arduino UNO, THD (Total Harmonic Distortion)

## I. INTRODUCTION

The project, titled "Design and Analysis of Hybrid Multilevel Inverter for Asymmetrical Input Voltage," aims to address the challenges associated with asymmetrical input voltages in power electronic systems. The proposed topology combines the strengths of traditional multilevel inverters with emerging technologies, creating a versatile solution for managing asymmetrical voltage scenarios.

Power electronic systems are crucial in various applications, but asymmetrical input voltages often impede their optimal functioning. While conventional multilevel inverters have been effective in mitigating certain issues, their ability to handle asymmetrical input voltages is limited. To overcome this limitation, the proposed topology integrates a hybrid configuration, merging cascaded H-bridge and flying capacitor multilevel inverters to create a robust and adaptable system.

The cascaded H-bridge inverter comprises multiple H-bridge cells connected in series, allowing for modularity and scalability. This arrangement enables the system to adjust to varying asymmetrical input conditions by selectively activating H-bridge cells to generate different voltage levels. The flying capacitor multilevel inverter introduces an additional layer of sophistication by using flying capacitors to bridge voltage gaps between levels, minimizing imbalances and enhancing stability.

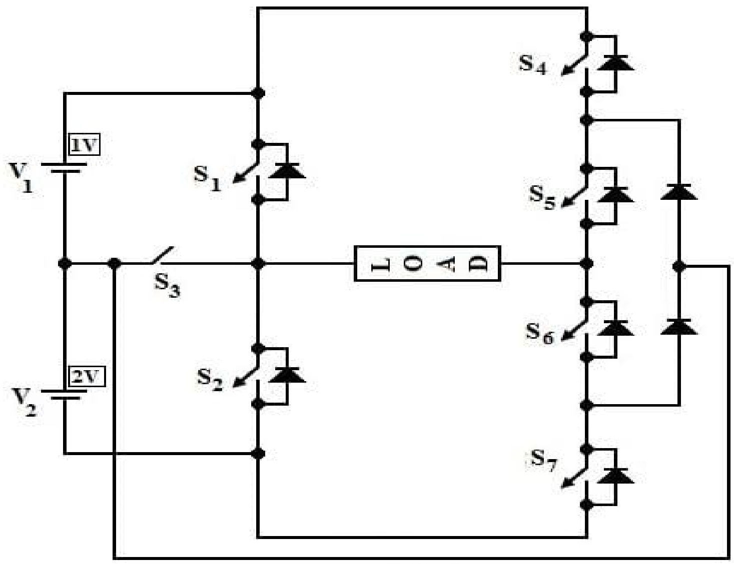


**FIGURE 1.** Generalized structure of proposed seven-level inverter topology.

A critical component of the proposed topology is the sophisticated control strategy, orchestrating the synchronized activation of H-bridge cells and flying capacitors. This strategy dynamically adjusts the modulation index and capacitor voltages, optimizing the inverter's performance under varying asymmetrical input conditions.

In Figure 1, the leg representing the three-level T-type portion is depicted with positive and negative dc rails 'm' and 'n' respectively and dc sources V1 and V2 with their corresponding source currents as iz1y (t) and iz2y (t) The project includes a comprehensive performance analysis, incorporating simulations and experimental studies to assess the system's response to asymmetrical input voltages. Factors such as harmonic distortion, efficiency, and voltage balancing are considered to validate the proposed topology's capability and showcase its superiority over traditional multilevel inverter configurations.

In conclusion, the project introduces a novel hybrid multilevel inverter topology designed to handle asymmetrical input voltages effectively. Through the integration of cascaded H-bridge and flying capacitor configurations, coupled with a robust control strategy, the proposed topology demonstrates promising potential for enhancing the reliability, efficiency, and adaptability of power electronic systems in the face of asymmetrical input voltage challenges. This research contributes valuable insights to the advancement of power electronics, paving the way for more resilient and high-performance energy conversion technologies.

## II. PROPOSED STRUCTURE

The proposed topology for the project, "Selective Harmonic Elimination Pulse Width Modulation-Based Hybrid Multilevel Inverter Topology with Reduced Components," is a sophisticated design that addresses the challenges of harmonic distortion and component count in power electronics that is shown in figure 1. The architecture combines cascaded H-bridge cells, flying capacitor cells, and innovative asymmetry in source configuration to achieve selective harmonic elimination (SHE) using pulse width modulation (PWM) techniques.

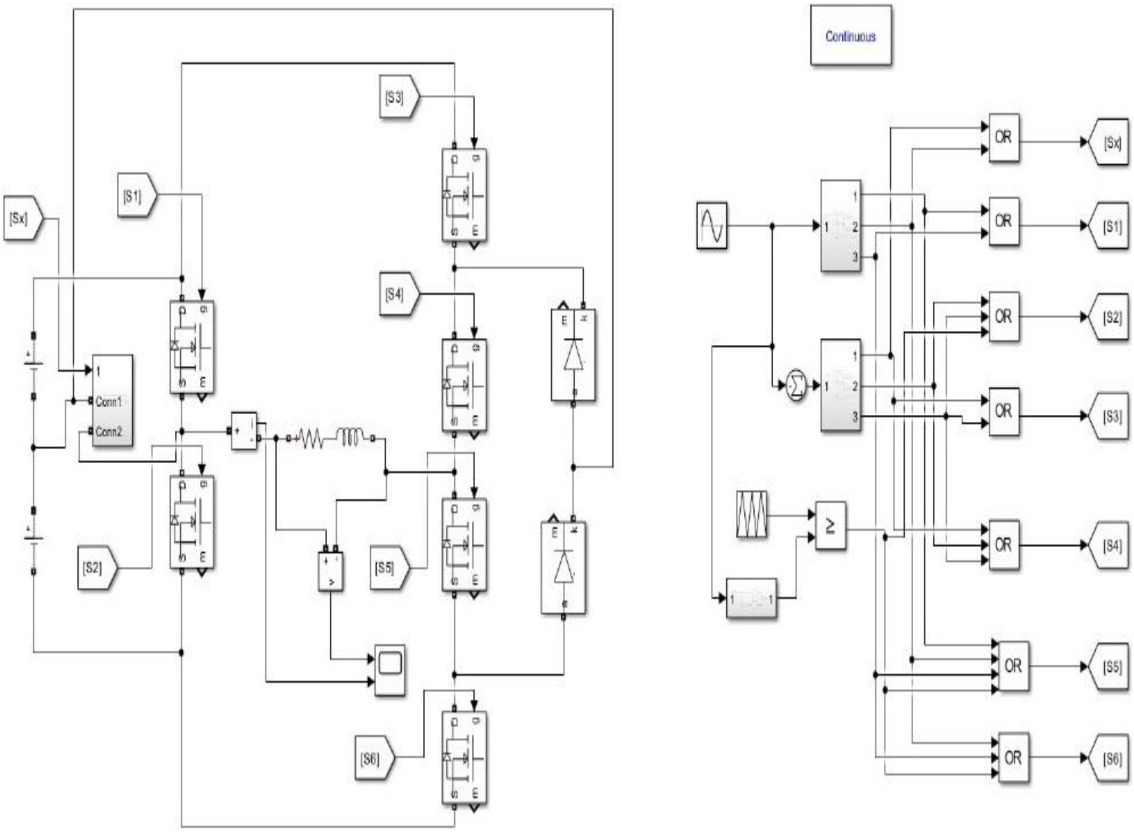


**Figure 2.** Simulation Diagram of 11 Level Inverter.

## Voltage Output Expression

The output voltage (Vout) of the hybrid multilevel inverter can be expressed as the sum of contributions from each H-bridge cell and flying capacitor cell

$$Vou\ t=\sum i=1nVi$$

## Harmonic Elimination Using SHE-PWM

Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) is implemented to minimize specific harmonics in the output waveform. The pulse width modulation is achieved through the adjustment of switch states, represented by the following equations for the duty cycle ($Di$) of each switch in the inverter:

$$Di=m_i/2^{mi}$$

Where $m_i$ is an integer that determines the number of voltage steps and is chosen to eliminate specific harmonics, As Figure 2.Represent Simulation Diagram of 11 stage Multilevel inverter using MATLAB software.

## Mathematical Model For Asymmetry

The proposed asymmetry in source configuration introduces modulation indices ($m_{asymi}$) to control the amplitudes of the input sources. These modulation indices are strategically adjusted to achieve the desired harmonic elimination while maintaining system stability

$$Vi=m_{asymi}.V_{DC}$$

Where $V_{DC}$ is the DC input voltage.

## Synthesis Parameter Optimization

Optimization of parameters such as capacitor values ($Ci$), switching frequencies ($f_{swi}$), and modulation indices is essential for achieving optimal performance. The synthesis involves adjusting these parameters to minimize harmonic distortion and enhance overall inverter efficiency.

## Switching Frequency Relationship

The switching frequencies of the H-bridge cells and flying capacitor cells are interrelated to avoid interference and maintain the integrity of the output waveform. The relationship between the switching frequencies is defined by

$$f_{swi} = nf_{swbase}$$

Where $f_{swbase}$ is the base switching frequency, and $n$ is an integer.

# III. PRINCIPLE OF SYNTHESIS

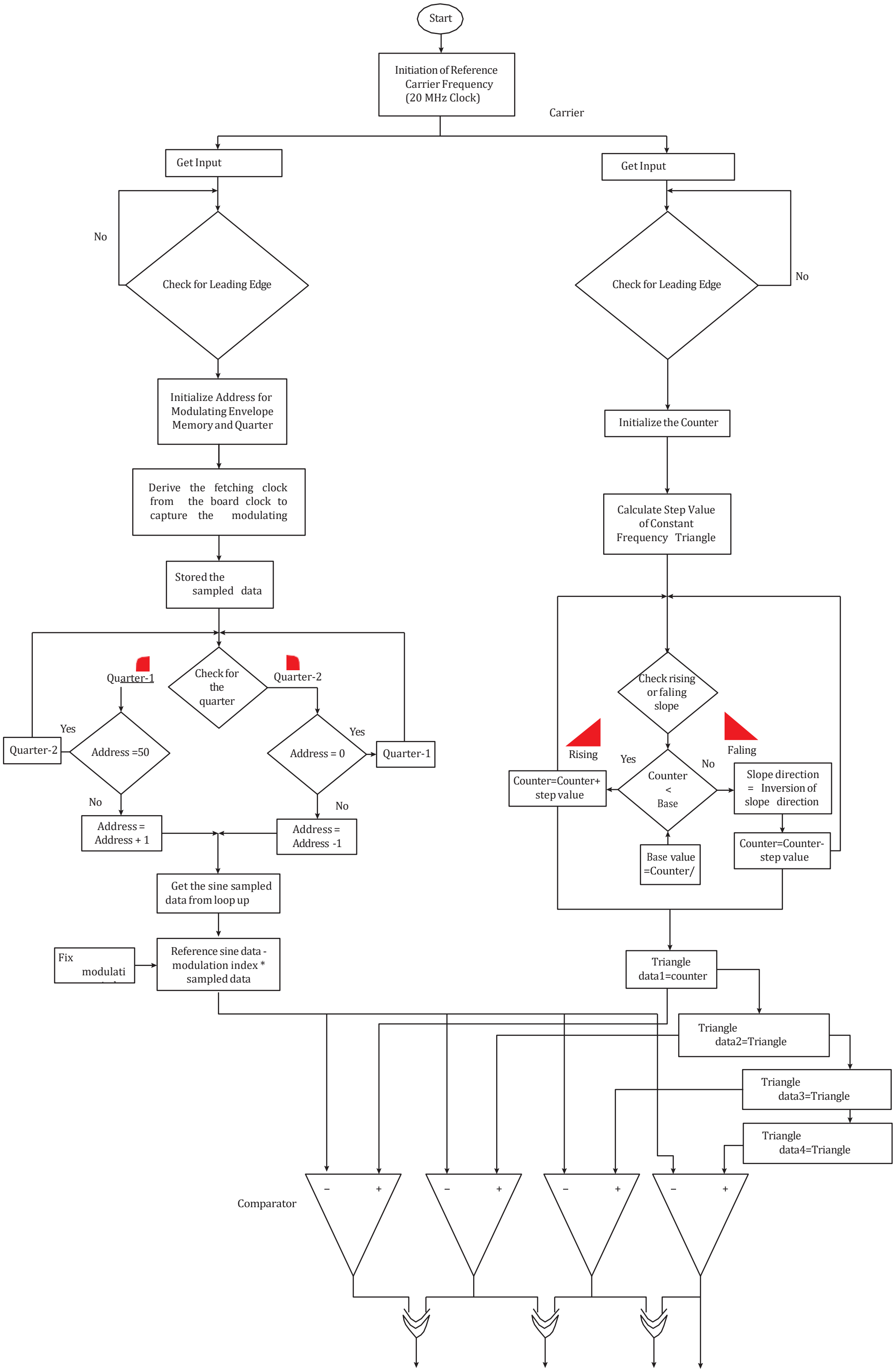


**FIGURE 3.** Experimental flow chart for FPGA pulse generation.

The principle of synthesis revolves around strategically combining cascaded H-bridge cells and flying capacitor cells to achieve multilevel voltage output to gating pulse generation avails UTs to synthesize the desired pulse train using the Xilinx Gating pulses for the switches (S1 to S8) in the switched confgured stage of the proposed topology to produce 9 level in the output voltage waveform Spartan 3E FPGA controller as portrayed in Figure 3.

The H-bridge cells provide stepped voltage levels, contributing to harmonic reduction, while flying capacitor cells enhance voltage control. The synthesis process optimizes parameters such as capacitor values, switching frequencies, and modulation indices to achieve the desired performance.

To optimize the synthesis, a careful selection of modulation indices ($m_{asymi}$) is required to introduce controlled asymmetry in the source configuration. These modulation indices control the amplitudes of the input sources and play a crucial role in achieving selective harmonic elimination.

### Proposed Asymmetry in Source Configuration

The innovative aspect of the proposed topology lies in introducing controlled asymmetry in the source configuration. This involves strategically adjusting the modulation indices ($m_{asymi}$) to induce imbalances in the input sources. The asymmetry is a deliberate design choice, allowing for a more refined control over harmonic content in the output waveform.

Mathematically, the asymmetry is represented by modifying the voltage contributions ($Vi$) as

$$Vi=m_{asymi}.V_{DC}$$

Where $V_{DC}$ is the DC input voltage, and $m_{asymi}$ is the modulation index for the $i$-th cell.

The controlled asymmetry not only aids in harmonic elimination but also contributes to a reduction in the overall component count. This reduction enhances the simplicity, reliability, and cost-effectiveness of the inverter system.

### Integration and Implementation

The proposed topology's methodology involves the integration of the synthesized design into a functional inverter system. This encompasses the physical implementation of H-bridge cells, flying capacitor cells, and the associated control circuitry. The SHE-PWM algorithm is implemented to dynamically adjust the switching states, ensuring the selective elimination of harmonics

## IV. ESTIMATION METHOD

### Enhancing Adaptability and Robustness

The estimation method within the proposed hybrid multilevel inverter topology represents a key advancement in achieving adaptability and robustness. This dynamic approach involves continuous adjustments to modulation indices based on real-time feedback from the inverter system and load conditions. Mathematically expressed as $m_i$=f (System Parameters, Load Conditions), this function dynamically tunes modulation indices to optimize the inverter's performance.

### Integration Into Synthesis Process

The synthesis process seamlessly incorporates the estimation method, aligning with the overarching principle of combining different converter configurations. This integration allows the inverter to dynamically respond to changes in load conditions, continuously adjusting modulation indices for optimal selective harmonic elimination. The dynamic nature of the estimation method ensures the inverter's adaptability, making it particularly valuable in applications with variable loads, such as renewable energy systems and motor drives.

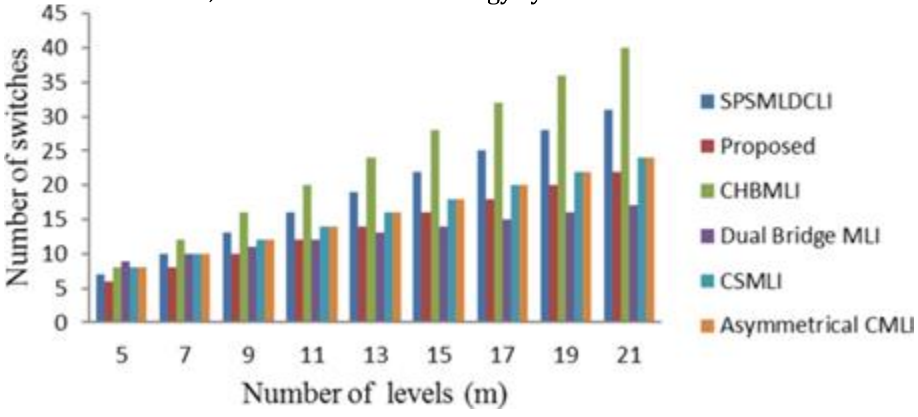


**FIGURE 4.** Topologies number of switches Versus Number of levels.

In Chong et al. (2008), From figure 4. a modular multilevel converter coupled with an H-bridge inverter has been used in the power conversion of the wind system. In this system, a transformerless wind energy conversion system (WECS) provided lightweight and analyzed power-sharing by asuitable switching strategy.

## Controlled Asymmetry: Harmonic Refinement

Within the estimation method, the proposed topology retains its distinctive feature of introducing controlled asymmetry in the source configuration. The dynamically adjusted modulation indices for asymmetry contribute to the refinement of harmonic content, further aligning with the estimation method's adaptability. This controlled asymmetry not only aids in harmonic elimination but also contributes to the reduction of the overall component count, enhancing the inverter's efficiency and versatility. The integration of the estimation method in figure 5. thus marks a significant step towards a more adaptive, robust, and efficient multilevel inverter system.

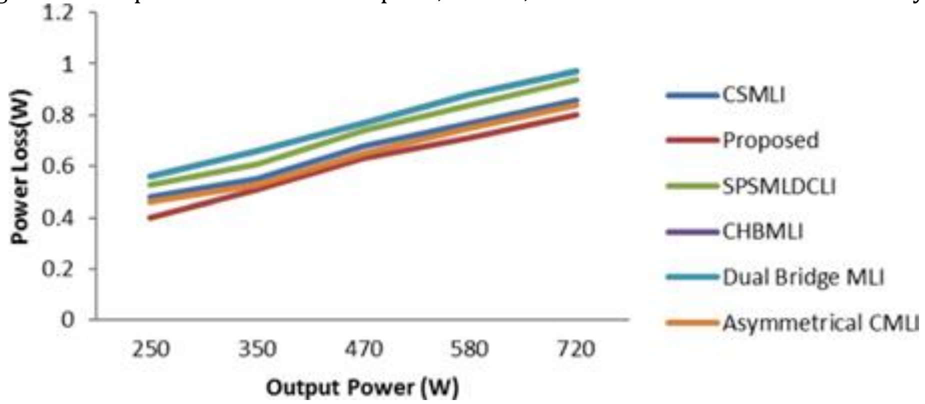


**FIGURE 5.** Topologies Power loss Versus Output power

# V. WORKING PRINCIPLE

## Cascaded H-Bridge Topology

The foundation of the HMI's working principle lies in the cascaded H-bridge topology. This configuration consists of multiple H-bridge cells connected in series. Each H-bridge cell independently contributes to the total output voltage, enabling the synthesis of a stepped waveform. The modularity of this topology facilitates improved voltage balancing and distribution, reducing the stress on individual switching devices. This inherent feature enhances the overall efficiency and reliability of the inverter.

## Flying Capacitor Topology

Complementing the cascaded H-bridge, the flying capacitor topology introduces capacitors to the system. These capacitors create additional voltage levels between the DC bus and the output. By adjusting the voltage across these flying capacitors, the inverter achieves multiple output voltage levels. This topology is known for its ability to enhance output waveform quality by mitigating harmonics and reducing Total Harmonic Distortion (THD).

## Hybrid Configuration

The distinctive feature of the HMI is its hybrid configuration, seamlessly integrating the cascaded H-bridge and flying capacitor topologies. This synergistic combination capitalizes on the benefits of both, addressing their individual limitations. The cascaded H-bridge provides flexibility and robustness in voltage control, while the flying capacitor topology contributes to improved output waveform quality. This synergy is particularly advantageous when handling asymmetrical input voltages.

## Handling Asymmetrical Input Voltages

Asymmetrical input voltages often result from irregularities in the power supply or grid conditions. The HMI's working principle equips it with the capability to effectively handle such scenarios. The individual control of H-bridge cells allows for adjustments to accommodate uneven input conditions. Moreover, the flying capacitor topology dynamically redistributes charge among capacitors, contributing to balanced voltage levels even in the presence of asymmetry.

## Voltage Balancing

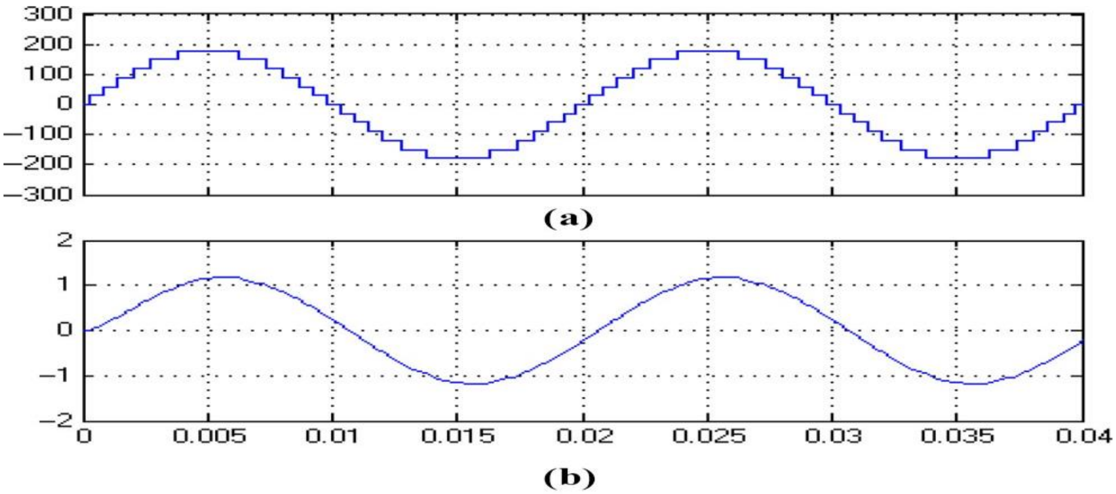
Maintaining balanced voltage levels across the inverter cells is crucial for reliable and efficient operation. The cascaded H-bridge topology, with its modular structure, facilitates individual control of each cell. This capability proves instrumental in adjusting the contribution of each cell to accommodate variations in input voltages. Simultaneously, the flying capacitor topology aids in voltage balancing by dynamically redistributing charge among the capacitors, ensuring a harmonious distribution of voltage levels.

## Control Algorithms

The effective operation of the HMI under asymmetrical input conditions relies on sophisticated control algorithms. Proportional-Integral (PI) controllers, pulse width modulation (PWM) techniques, and advanced modulation schemes are employed in the control system. These algorithms continually monitor the input voltages and dynamically adjust the switching states of the inverter cells to maintain the desired output waveform and optimal performance.

## VI. SIMULATION RESULTS

The simulation results of the Hybrid Multilevel Inverter for Asymmetrical Input Voltage demonstrate its efficacy in handling uneven input conditions that we could clearly notice in figure 6. The output waveform exhibits reduced Total Harmonic Distortion (THD) and improved voltage balance, showcasing the benefits of the integrated cascaded H-bridge and flying capacitor topologies as shown in figure 6. The inverter maintains stable operation even when subjected to asymmetrical voltage scenarios, validating its suitability for real-world applications. These results affirm the successful design and functionality of the proposed hybrid inverter, emphasizing its potential for enhancing power system performance in environments with varying and asymmetrical input voltages.



**Notes:** (a) Output voltage; (b) inductive load current

**Figure 6.** Load voltage and current waveform of proposed multilevel inverter

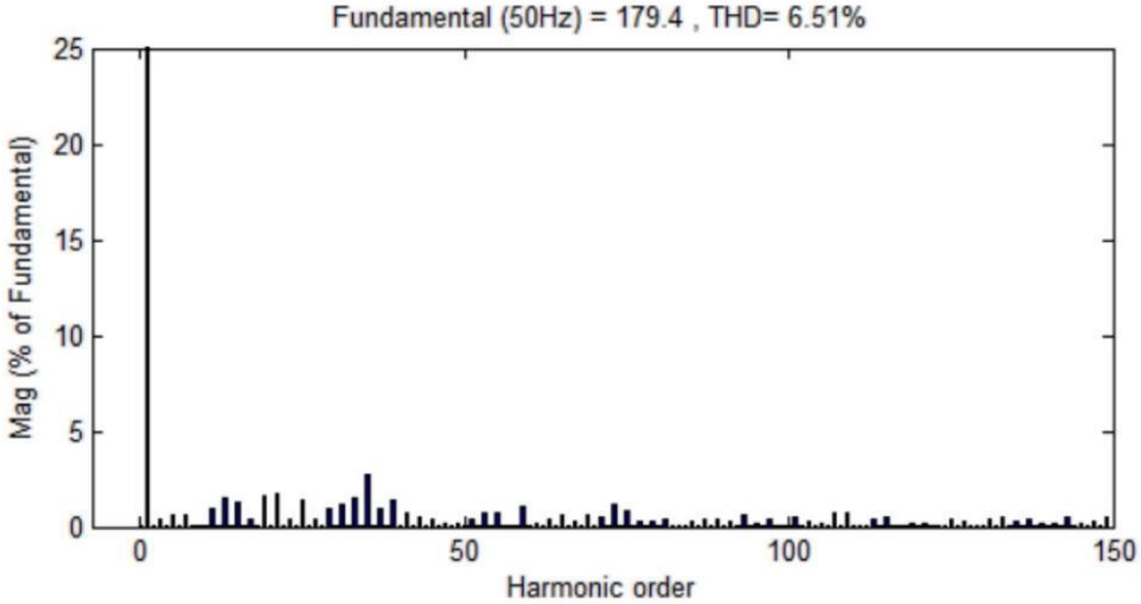


**Figure 7.** 11-level proposed asymmetrical sub-MLI

## VII. FUTURE SCOPE

### Scalability for Higher Power Applications

As technology progresses, the Hybrid Multilevel Inverter (HMI) presents a promising avenue for exploration in terms of scalability. Future research can focus on optimizing design parameters to accommodate higher voltage and current levels, expanding the applicability of the HMI to a wider range of industrial and renewable energy systems. This evolution would contribute to meeting the growing demand for power electronics solutions capable of handling larger power capacities with enhanced efficiency.

### Integration of Advanced Semiconductor Devices

The future of the HMI involves leveraging advanced semiconductor devices and materials. Exploring wide-bandgap semiconductors like silicon carbide (SiC) and gallium nitride (GaN) holds potential for significantly improving the inverter's efficiency and switching speed. The incorporation of these materials can reduce power losses, making the HMI a more sustainable and environmentally friendly solution. This avenue of research aligns with the broader industry trend towards adopting cutting-edge materials in power electronics.

### Intelligent and Adaptive Control Strategies

Advancements in control algorithms are pivotal for the future development of the HMI. Applying machine learning and artificial intelligence techniques can optimize the inverter's response to varying input conditions. Intelligent and adaptive control systems can anticipate and dynamically adjust to asymmetrical input voltage scenarios, enhancing the overall robustness and adaptability of the HMI. This approach aligns with the ongoing trend of incorporating smart and autonomous features into power electronics systems.

### Integration with Energy Storage and Smart Grid Technologies

The future holds significant opportunities for integrating the HMI with energy storage systems and smart grid technologies. Researchers can explore the incorporation of energy storage elements, such as batteries or supercapacitors, to store and release energy strategically. This integration can mitigate fluctuations caused by asymmetrical inputs and contribute to grid resilience. Additionally, the adaptability of the HMI to smart grid architectures can play a vital role in developing more resilient and responsive power distribution networks, supporting the transition towards sustainable and decentralized energy systems.

## VII. CONCLUSION

[1] The project concludes by validating the effectiveness of the designed hybrid multilevel inverter in accommodating asymmetrical input voltage conditions.[2] Through advanced control strategies and modulation techniques, the project demonstrates optimized performance of the multilevel inverter under varying input voltage scenarios.[3] The practical relevance of the designed multilevel inverter is highlighted, showcasing its potential for deployment in real-world industrial settings with prevalent asymmetrical input voltages.[4] The multilevel inverter's robust control algorithms enable effective management of asymmetrical voltage fluctuations in renewable energy systems.

[5]Integrating the latest advancements in power semiconductor devices improves the efficiency and reliability of the multilevel inverter. [6]Accurate modelling and simulation methodologies are crucial in analysing the multilevel inverter's performance and guiding future design iterations.:[7] The multilevel inverter plays a crucial role in stabilizing grid operations, particularly in scenarios involving asymmetrical input voltages from solar arrays. [8]Multilevel inverters contribute significantly to advancing renewable energy integration and enhancing grid stability for a more sustainable energy infrastructure.

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