An Efficient Switch-Capacitor Charge Pump for Enhanced PLL Performance in 5G Transceivers

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***Abstract*— The fifth generation of cellular technology (5G) aims to revolutionize connectivity by enabling a broad spectrum of uses including augmented reality, autonomous vehicles, and the Internet of Things (IoT). Charge Pump (CP) is a critical component of phase-locked loops (PLLs), particularly in 5G transceivers, where it plays a pivotal role in adjusting the voltage-controlled oscillator (VCO) frequency based on phase error. The current mismatch presents a significant challenge in CP design, potentially leading to PLL loss of lock. To address this issue, researchers worldwide have explored various circuitry solutions, often resulting in bulky and power-intensive implementations. In this study, a switch-capacitor-based CP is designed using 90 nm CMOS technology. The designed CP achieves remarkably low power consumption of only 17.38 µW, with an impressively low current mismatch of 0.034%. These findings underscore the potential of our CP design to enhance PLL performance, offering a promising solution for demanding high-performance applications.**

Keywords*— *CMOS, PLL, Transceiver, RF

I. INTRODUCTION

The fifth generation (5G) of cellular technology offers notably swifter data speeds, reduced latency, and expanded capacity in contrast to its forerunners. 5G is essential for transforming connectivity and enabling diverse applications like augmented reality, autonomous vehicles, the Internet of Things (IoT), and more. However, designing CMOS circuits for 5G applications presents several challenges. Firstly, the high-frequency operation required by 5G systems demands CMOS circuits with high-speed performance and low power consumption. Achieving these requirements while maintaining signal integrity and minimizing interference is challenging. Additionally, 5G systems often involve complex signal processing algorithms and massive MIMO (Multiple Input Multiple Output) configurations, requiring advanced CMOS designs capable of handling large amounts of data with high efficiency. Moreover, the deployment of 5G networks requires CMOS designs that are cost-effective and scalable to meet the growing demands of the market. Overall, addressing these challenges is essential for realizing the full potential of 5G communication and advancing the capabilities of wireless technology.

Complementary Metal-Oxide-Semiconductor (CMOS) technology stands as a cornerstone in modern electronics, particularly in the realm of analog device design. It comprises a fundamental integrated circuit (IC) fabrication technique where both n-type and p-type metal-oxide-semiconductor field-effect transistors (MOSFETs) coexist on a single chip, offering low power consumption, high noise immunity, and scalability [1]. Researchers favor CMOS for analog device design owing to its ability to integrate various analog and digital functions on the same chip, facilitating enhanced performance, reduced footprint, and lower production costs. Furthermore, CMOS technology enables the implementation of advanced signal processing techniques, making it a preferred choice for developing cutting-edge analog devices across a spectrum of applications, from telecommunications to medical instrumentation [1].

In numerous applications spanning telecommunications, data communications, frequency synthesis, clock recovery, and signal demodulation phase-locked loops (PLLs) are extensively employed [2]. Fig. 1 presents the block diagram of a typical PLL. At its core, a PLL synchronizes the phase and frequency of an output signal with those of a reference signal, ensuring precise timing and frequency control. The major components of a PLL typically include a phase detector, a charge pump, a voltage-controlled oscillator (VCO) [3], and a loop filter. The phase detector compares the phase of the feedback signal from the output with the reference signal, generating an error signal. This error signal is then converted to the current signal by the charge pump (CP). This current signal, after filtering by the loop filter, adjusts the voltage applied to the VCO, thereby locking the VCO's output frequency to that of the reference signal. This closed-loop system ensures stable and accurate frequency and phase synchronization, making PLLs indispensable in modern communication systems, data storage devices, and various other electronic systems requiring precise timing and frequency control.

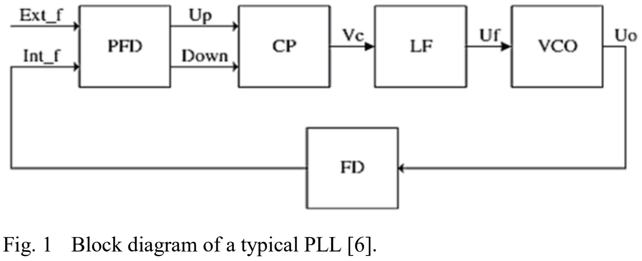

Fig. 1 Block diagram of a typical PLL [6].

A charge pump is a fundamental electronic circuit used for generating a higher voltage from a lower voltage source by utilizing the principles of capacitor charging and discharging. It operates by periodically transferring charge from an input voltage source to an output voltage node, typically through a series of switches and capacitors. Charge pumps find widespread application in various electronic systems, including voltage converters, voltage multipliers, and power management circuits, due to their simplicity, efficiency, and ability to provide voltage boosting without the need for inductors.

Huili et al. (2012) [4] proposed a charge pump (CP) design that employs a double-ended output amplifier to enhance current matching. The op-amp ensures equal voltage between two specific nodes, thereby reducing current mismatch in the circuit. In another op-amp-based CP design [5], the op-amp is used for compensation, effectively minimizing current mismatch by precisely matching the up and down currents. While these op-amp-based CP designs significantly reduce current mismatch, they also increase die area and power consumption due to the added circuitry. Additionally, these designs do not offer any features to improve the locking time of the PLL. Therefore, an optimized CP design is needed that minimizes power consumption and die area while also contributing to the reduction of PLL locking time.

II. METHODOLOGY

The charge pump plays a pivotal role in PLL, converting the phase error signal from the phase frequency detector (PFD) into a current signal. Later, the loop filter converts the current signal to control voltage and is used to modify the oscillator's frequency. Generally, CPs have two modes: charge and discharge. When the charge pump is operating in charge mode, the charge is pumped into a filter capacitor, producing a positive control voltage. The oscillator's frequency is raised by using this positive voltage. The filter capacitor is connected to the supply voltage or ground by the charge pump via a MOSFET or a diode, respectively. When the charge pump is in discharge mode, the filter capacitor's charge is purged, producing a negative control voltage. The oscillator's frequency is lowered with the help of this negative voltage.

The core component of the CP is the switched capacitor, also referred to as the basic CP module. In idle mode, both the 'UP' and 'DN' signals are low, resulting in PM0 and NM0 being on, which charges the capacitor C_v to VDD. When the PFD detects that the reference frequency is higher than the feedback frequency, it generates a high "UP" signal, putting the CP in a charging state. This "UP" signal activates PM1 and NM1, allowing C_v to charge the loop filter through these transistors. Conversely, when the PFD detects that the reference frequency is lower than the feedback frequency, it generates a "DN" signal, prompting the CP to enter a discharging state. In this state, the "DN" signal causes the loop filter to discharge through PM2, NM2, and C_v, reducing the voltage and frequency of the VCO. Fig. 2 shows the basic charging module of the CP.

Distortions in a PLL may occur due to fluctuations in current during the charging and discharging phases. To mitigate these fluctuations, precise tuning is crucial. During charging, the loop filter is charged through PM1 and NM1 of the basic switch-capacitor CP, while during discharging, it is discharged through PM2 and NM2. Fine-tuning the resistance of these MOSFETs enables control over current flow in both phases. Here VDD is the source voltage, Vt is the threshold voltage and Vgs is the gate voltage of the MOSFET. By adjusting Ron for NM1, PM1, NM2, and PM2, the charging and discharging currents can be regulated to minimize mismatch. This meticulous adjustment is essential for maintaining PLL stability and performance.

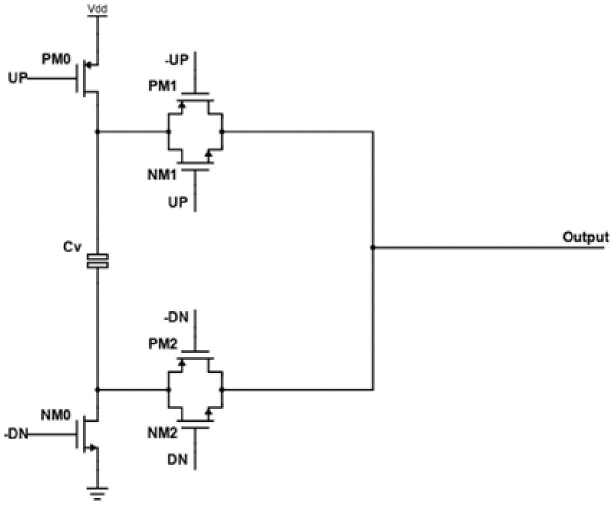

Fig. 2 Schematic diagram of the proposed switched-capacitor-based CP

III. RESULTS AND DISCUSSION

In this section, a detailed analysis of the charging and discharging of the CP is provided. The performance parameters of the proposed CP, such as current mismatch, tuning voltage, and power consumption, can be determined by using the following simulations and plots. The proposed CP and loop filter converts the "UP" signal into a voltage signal so VCO can account for the changed voltage. Fig. 3 and Fig. 4 represent the CP's charging and discharging timing diagram, respectively. For the transient analysis of the charging, the "UP" terminal of the CP is equipped with a square wave periodic signal with a period of 2 ns with a pulse width of 0.1 ns, and the "DN" terminal is kept at 0 V during this simulation. For the discharging simulation, the "DN" terminal of the CP is equipped with a square wave periodic signal with a period of 2 ns with a pulse width of 0.1 ns while keeping the UP at 0 V. During the transient simulation of discharging an initial condition of 1.2 V is used at the output node.

The current mismatch is a major issue while designing a CP. It is the difference between the charging and discharging current for a specific voltage. It causes the output voltage to charge or discharge quickly. As a result, the CP can lose its linearity, and the PLL may not be able to achieve the locking condition. To attain the current mismatch of the proposed CP, a transient analysis is performed to determine the charging and discharging current for various voltage levels. After achieving the charging and discharging current manually from the transient simulation, the current mismatch percentage is calculated for different voltage points. Fig. 5 presents the current mismatch plot of the proposed CP. The CP achieved a current mismatch of 0.034% from 0.2 to 1 V. The proposed CP also has a very low power consumption of only 17.38 μW.

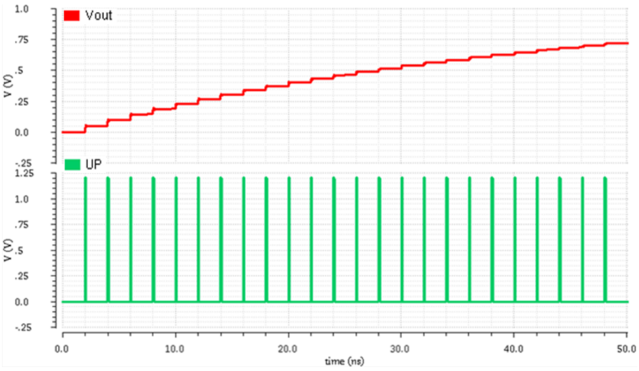

Fig. 3 Transient analysis of the basic charging of the proposed CP

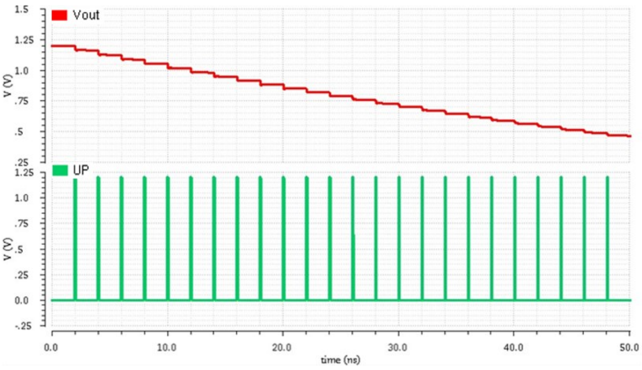

Fig. 4 Transient analysis of basic discharging of the proposed CP

The performance comparison of the suggested design and current CP efforts is presented in Table I. The switching method used in the suggested CP only calls for two capacitors and six MOSFETs. In addition to the switching method, an accelerated charging/discharging method is used to shorten the PLL's locking time. Eight MOSFETS and two capacitors are needed for the accelerated modules. There are just 14 MOSFETs and 4 capacitors needed for the entire CP architecture. The current mismatch that arises from the fluctuation in the charging and discharging currents is a significant consideration in the design of a CP. The device experiences nonlinearity due to the present CP mismatch, which might result in the PLL's locking state being lost. The current mismatch is decreased by optimizing the four MOSFETs through which charging and discharging current travels by using the W/L ratio optimization approach. The CP achieved a current mismatch of just 0.034% in the 0.2 to 1 V range using the optimization approach. Other researchers used other circuitry or op-amps to alleviate the current imbalance, although this significantly increased the devices' power consumption. The CP has the lowest power consumption of all the designs under study, at just 17.38 µW, thanks to the small number of components utilized in the circuits. This reduction in power consumption has occurred exponentially. The goal of achieving low power consumption power generation is effectively accomplished with low power consumption.

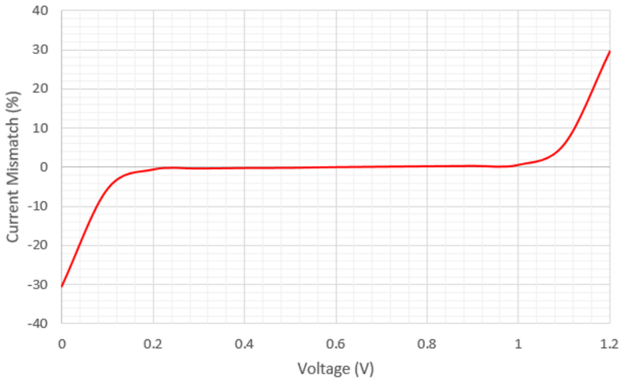

Fig. 5 Plot of current mismatch percentage of the proposed CP

TABLE I. PERFORMANCE COMPARISON OF THE PROPOSED CP WITH RECENT WORKS

Ref	**Topology**	**Process (nm)**	**Voltage Range (V)**	**Power Source (V)**	**Current variation**	**Power Consumption (µW)**
[6]	Cascode Current Mirror	180	0.4-1.25	1.8	0.065 %	3000
[7]	Adaptive Body Bias	180	0.2-1	1.2	0.9 %	-
[4]	Op-amp	180	0.4-1.7	1.8	0.05%	558
[5]	Op-amp	90	0-1.2	1.2	0.3%	134.7
[8]	Programmable	90	0.2-0.85	1	<1%	713
[9]	Bulk Driven	180	0.3-1.58	1.8	<1%	395
[10]	Mismatch Compensation	65	0.5-0.75	1	4%	360
This Work	Switching	90	0.2-1	1.2	0.034%	17.38

IV. CONCLUSION

In conclusion, the development of a switch-capacitor-based Charge Pump in this research represents a significant advancement in PLL design for 5G transceivers. By effectively addressing the challenge of current mismatch through innovative circuitry implemented in 90 nm CMOS technology, we have achieved remarkable results, including low power consumption and minimal current mismatch.

These findings underscore the potential of our CP design to significantly enhance the performance and efficiency of PLLs in 5G communication systems. Furthermore, the success of our approach highlights the importance of continued research and innovation in overcoming key challenges in RF circuit design, paving the way for further advancements in next-generation wireless communication technologies.

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